Semiconductor switch ratings have limited the application of power converters rated in the tens to hundreds of megawatts. Large inverters operating at these power levels in the medium voltage range (2-13 kV) have traditionally been the domains of gate turn off (GTO) thyristors. However, their switching speed is severely limited compared to the IGBT's so that the carrier frequency of a GTO inverter is generally only a few hundred hertz. High switching frequencies can be achieved by replacing each of the slower switches so that each individual IGBT shares the dc link voltage with others in the string during its off state. The devices are operated in saturation region of operation. This is because there exists higher losses in active region operation of these devices.

Minimum voltage and current harmonics.

Controlled neutral point voltage and current to ensure stiff capacitor voltages.

To obtain steps in the output voltage.

A three-level diode clamped inverter is shown in Figure 4.1. In this circuit, the dc bus voltage is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle point of the two capacitors “2” can be defined as the neutral point. The output voltage has three states: $V_{dc}/2$, 0, $-V_{dc}/2$. The devices are switched in combinations to obtain these levels in the voltage waveform. The switching combination of the top two ..is20007 T14

The output phase voltage of the inverter is given by

$$v_{ao} \quad H_{a3}V_{30} \quad H_{a2}V_{20} \quad H_{a1}V_{10} \tag{4.1}$$

$$v_{bo} \quad H_{b3}V_{30} \quad H_{b2}V_{20} \quad H_{b1}V_{10} \tag{4.2}$$

$$v_{co} \quad H_{c3}V_{30} \quad H_{c2}V_{20} \quad H_{c1}V_{10}\,. \tag{4.3}$$

The switches are assumed ideal as is common in preliminary functional analysis of switching power converters. These assumptions include: (a) negligible forward voltage drop of the switch throws in their on-state; (b) sufficient on-state current carrying capacity and of-state voltage blocking capacity commensurate and compatible with the voltage and current ratings of the system; and (c) negligible transition periods between turn on and turn off of the switch throws that permit repetitive high frequency switching. The voltages at the throw terminals of the switch are assumed stiff such that their variations during a switching period can be neglected. Similarly, the switch currents are assumed stiff such that their variations over a switching period can be neglected. These assumptions essentially allow the focus to be on the power transfer process and the functional features. In practical power converters, filter elements appropriately applied at the input and output ports of the system would ensure that these assumptions are valid. In order to maintain continuity of the three phase currents connected to the poles, at least one of the throws connected to any given pole of the switch has to be closed. Furthermore, each current port may be connected to only one voltage terminal at any given instant of time. Otherwise, two stiff voltages will be short-circuited together, resulting in uncontrolled currents through the switch throws. As a result, no more than one combination of switches is on at any given instant of time. Hence the following conditions are to be followed when switching the devices of a multilevel converter.

$$H_{a3} \quad H_{a2} \quad H_{a1} \quad 1 \tag{4.4}$$

$$H_{b3} \quad H_{b2} \quad H_{b1} \quad 1 \tag{4.5}$$

$$_{3} \quad _{2} \quad _{1} \quad 1$$

Writing the Kirchoff's Current Law (KCL) equation at node 3 gives the differential equation of the capacitor voltage V_{c1} and KCL equation at node 1 gives differential equation for capacitor voltage V_{c2}.

$$C_1 pV_{c1} \quad I_{dc} \quad H_{a3} i_a \quad H_{b3} i_b \quad H_{c3} i_c . \tag{4.14}$$

$$C_2 pV_{c2} \quad I_{dc} \quad H_{a1} i_a \quad H_{b1} i_b \quad H_{c1} i_c \quad . \tag{4.15}$$

Multilevel converters can be modulated using the following two methods:

Direct digital technique SVPWM.

Carrier-based (triangular comparison) technique.

The direct digital technique involves utilization of space vector approach wherein the duty cycles for the switching inverter are calculated. The gating signals are

scheme, single carrier waveform and N modulation signals are used. The concept of sharing functions is introduced in this section.

The output voltages of the three level inverter is defined by the following equations

$$3\ 30 \qquad 2\ 20 \qquad H\ _1V_{10}$$

The above objective function has to be minimized subject to the six constraint equations mentioned above.

Writing the six equations in the matrix form,

2

1

3

2

1

The optimized solution of the matrix (4.19) is given by

$$X = Z\,A^{T}\,[A\,Z\,A^{T}]^{-1}\,Y. \qquad (4.27)$$

where Z is given by

$$\begin{matrix}
\frac{1}{K_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{1}{K_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & \frac{1}{K_3} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & \frac{1}{K_4} & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{1}{K_5} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & \frac{1}{K_6} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_7} & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_8} & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{K_9}
\end{matrix} .$$

In the present case consider

$$K_1 \quad K_4 \quad K_7$$

$$K_2 \quad K_5 \quad K_8$$

$$K_3 \quad K_6 \quad K_9.$$

In the above mentioned assumption, say $K_1 = K_4 = K_7$, it states that the sharing function corresponding to the top devices in all the three phases is equal and correspondingly the remaining assumptions are for the other devices.

Hence the solution to the objective function gives the expressions for the switching functions.

2 2

3 2 3 1 3 2 2 3 1 2

$$H_{a3} \quad \frac{2v_{a0}}{3V_d} \quad \frac{1}{3} \qquad H_{b3} \quad \frac{2v_{b0}}{3V_d} \quad \frac{1}{3} \qquad H_{c3} \quad \frac{2v_{c0}}{3V_d} \quad \frac{1}{3} \tag{4.36}$$

$$H_{a2} \quad \frac{1}{3} \qquad H_{b2} \quad \frac{1}{3} \qquad H_{c2} \quad \frac{1}{3} \tag{4.37}$$

$$H_{a1} \quad \frac{2v_{a0}}{3V_d} \quad \frac{1}{3} \qquad H_{b1} \quad \frac{2v_{b0}}{3V_d} \quad \frac{1}{3} \qquad H_{c1} \quad \frac{2v_{c0}}{3V_d} \quad \frac{1}{3}. \tag{4.38}$$

The pattern of switching for the switching devices used in converter is periodic; therefore the analysis of the switching functions is simple by using the Fourier series. Thus the switching pulses can be represented as sum of dc component and fundamental component either sine or cosine varying term. It can be assumed as

$$H_{a3} \quad \frac{1}{3} 1 \quad M_{a3} \tag{4.39}$$

$$H_{a2} \quad \frac{1}{3} 1 \quad M_{a2} \tag{4.40}$$

$$H_{a1} \quad \frac{1}{3} 1 \quad M_{a1} \tag{4.41}$$

where M_{a3}, M_{a2}, M_{a1} are called the modulation signals, which can be cosine or sine term. These signals represent the fundamental component of the switching pulses. When this fundamental component is compared with the high frequency carrier waveform produces the same pattern of the pulses.

By comparing Eqs. (4.39 – 4.41) with Eqs. (4.36 – 4.38), the modulation signals are obtained as

$$M_{a3} \quad \frac{2v_{a0}}{V_d}$$

The node currents of the inverter are given by

$$I_3 \quad H_{a3} i_a \quad H_{b3} i_b \quad H_{c3} i_c \tag{4.43}$$

$$I_2 \quad H_{a2} i_a \quad H_{b2} i_b \quad H_{c2} i_c \tag{4.44}$$

$$I_1 \quad H_{a1} i_a \quad H_{b1} i_b \quad H_{c1} i_c . \tag{4.45}$$

Writing the KCL equation at node 3 gives the differential equation of the capacitor voltage V_{c1} and KCL equation at node 1 gives differential equation for capacitor voltage V_{c2}.

$$C_1 p V_{c1} \qquad I_{dc} \quad H_{a3} i_a \quad H_{b3} i_b \quad H_{c3} i_c \tag{4.46}$$

$$C_2 p V_{c2} \qquad I_{dc} \quad H_{a1} i_a \quad H_{b1} i_b \quad H_{c1} i_c$$

(a)

(b)

(c)

Figure 4.3: Simulation results of three-level inverter using the single carrier-based technique (I) (a), (b), (c) Three-phase voltages (II) three-phase currents

Using the modulation signals that are obtained using Eq. (4.42), the carrier-based PWM is implemented. Figure 4.3 illustrates the simulation results for a three-level inverter, which is modulated using the single carrier-based PWM technique. Figure 4.3 (I) (a), (b), (c) shows the three-phase voltages generated. Figure 4.3 (II) gives the three-phase currents generated when the voltages are impressed across a balanced three-phase load.

The output voltages of the four-level inverter is defined by the following equations.

$$v_{ao} \quad H_{a4}V_{40} \quad H_{a3}V_{30} \quad H_{a2}V_{20} \quad H_{a1}V_{10} \tag{4.48}$$

$$v_{bo} \quad H_{b4}V_{40} \quad H_{b3}V_{30} \quad H_{b2}V_{20} \quad H_{b1}V_{10} \tag{4.49}$$

$$v_{co} \quad H_{c4}V_{40} \quad H_{c3}V_{30} \quad H_{c2}V_{20} \quad H_{c1}V_{10} \tag{4.50}$$

The switching constraints to be followed in order to avoid the shorting of the dc bus voltage source are

$$H_{a4} \quad H_{a3} \quad H_{a2} \quad H_{a1} \quad 1 \tag{4.51}$$

$$H_{b4} \quad H_{b3} \quad H_{b2} \quad H_{b1} \quad 1 \tag{4.52}$$

$$H_{c4} \quad H_{c3} \quad H_{c2} \quad H_{c1} \quad 1. \tag{4.53}$$

There are six equations and 12 unknowns (H_{a4}, H_{b4}, H_{c4} … H_{c1}), the set of equations has an indeterminate solution. The optimization technique used in case of three-level is extended to four-level to obtain the solution, which minimizes the sum of zes the s63 n

Writing the six equations in the matrix form,

$$H_{a4} \quad \frac{3v_{a0}}{4V_d} \quad \frac{1}{4} \qquad H_{b4} \quad \frac{3v_{b0}}{4V_d} \quad \frac{1}{4} \qquad H_{c4} \quad \frac{3v_{c0}}{4V_d} \quad \frac{1}{4} \tag{4.56}$$

$$H_{a3} \quad \frac{v_{a0}}{4V_d} \quad \frac{1}{4} \qquad H_{b3} \quad \frac{v_{b0}}{4V_d} \quad \frac{1}{4} \qquad H_{c3} \quad \frac{v_{c0}}{4V_d} \quad \frac{1}{4} \tag{4.57}$$

$$H_{a2} \quad \frac{v_{a0}}{4V_d} \quad \frac{1}{4} \qquad H_{b2} \quad \frac{v_{b0}}{4V_d} \quad \frac{1}{4} \qquad H_{c2} \quad \frac{v_{c0}}{4V_d} \quad \frac{1}{4} \tag{4.58}$$

$$H_{a1} \quad \frac{3v_{a0}}{4V_d} \quad \frac{1}{4} \qquad H_{b1} \quad \frac{v_{b0}}{4V_d} \quad \frac{1}{4} \qquad H_{c1} \quad \frac{3v_{c0}}{4V_d} \quad \frac{1}{4}. \tag{4.59}$$

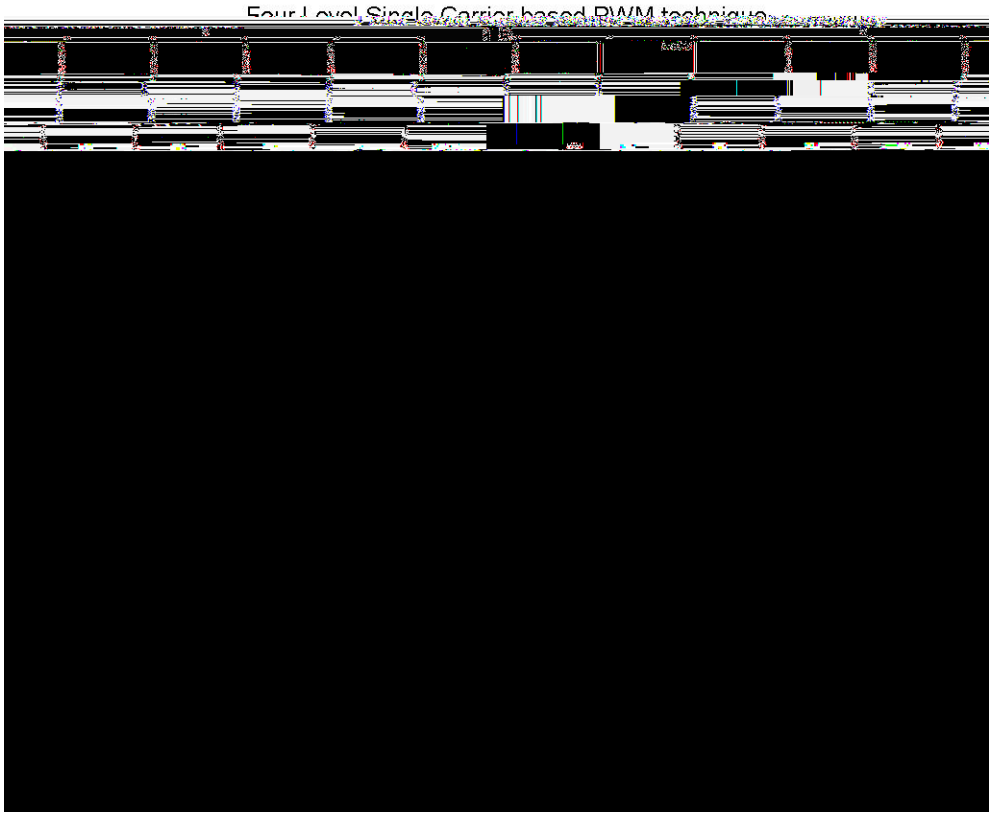


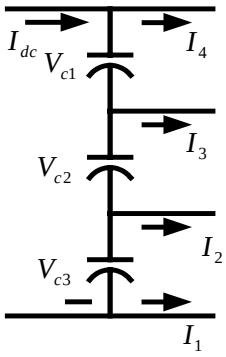
Figure 4.4: Single Carrier and Multiple Modulation Signal PWM Technique for a Four-Level Inverter

The node currents of the inverter are given by

$$I_4 \quad H_{a4} i_a \quad H_{b4} i_b \quad H_{c4} i_c \tag{4.65}$$

$$I_3 \quad H_{a3} i_a \quad H_{b3} i_b \quad H_{c3} i_c \tag{4.66}$$

$$_{a\ a} \quad _{b\ b} \quad _{c}$$


I_{dc}
V_{c1}
I_4
I_3
V_{c2}
I_2
V_{c3}
I_1

$$H_{a5} \quad H_{a4} \quad H_{a3} \quad H_{a2} \quad H_{a1} \quad 1 \tag{4.75}$$

$$H_{b5} \quad H_{b4} \quad H_{b3} \quad H_{b2} \quad H_{b1} \quad 1 \tag{4.76}$$

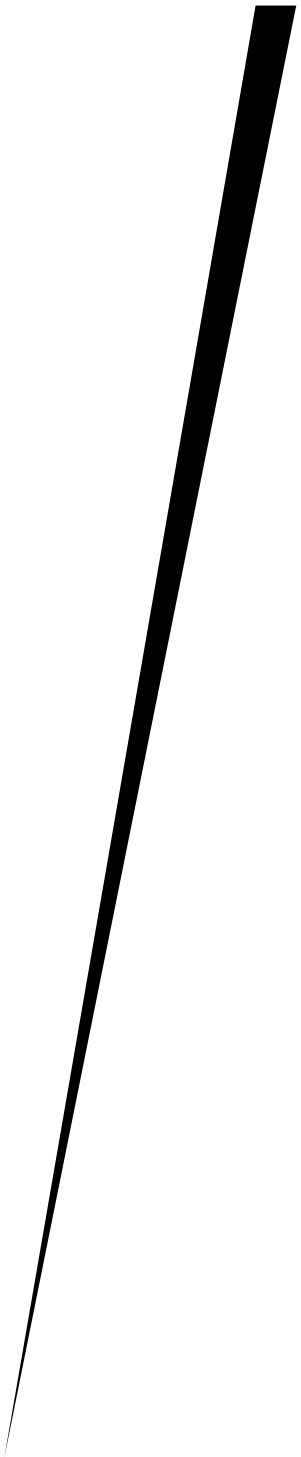
$$H_{c5} \quad H_{c4} \quad H_{c3} \quad H_{c2} \quad H_{c1} \quad 1. \tag{4.77}$$

There are six equations and fifteen unknowns (H_{a5}, H_{c5}, H_{b5} … H_{c1}); the set of equations has an indeterminate solution. Optimization technique is used to obtain the

The optimized solution of the above matrix is given by

$$X = Z\,A^{T}\,[A\,Z\,A^{T}]^{-1}\,Y$$

where Z is given by



Assuming the following,

$$K_1 \quad K_6 \quad K_{11}$$

$$K_2 \quad K_7 \quad K_{12}$$

$$K_3 \quad K_8 \quad K_{13}$$

$$K_4 \quad K_9 \quad K_{14}$$

$$K_5 \quad K_{10} \quad K_{15}.$$

By substituting the above assumption and solving the matrix gives the expressions for the modulation signals [A.2]. Substituting the above steady state values and assuming all the sharing functions to be equal to be unity, the modulation signals are obtained as

$$H_{a5} \quad \frac{4v_{a0}}{5V_d} \quad \frac{1}{5} \qquad H_{b5} \quad \frac{4v_{b0}}{5V_d} \quad \frac{1}{5} \qquad H_{c5} \quad \frac{4v_{c0}}{5V_d} \quad \frac{1}{5} \tag{4.79}$$

$$H_{a4} \quad \frac{2v_{a0}}{5V_d} \quad \frac{1}{5} \qquad H_{b4} \quad \frac{2v_{b0}}{5V_d} \quad \frac{1}{5} \qquad H_{c4} \quad \frac{2v_{c0}}{5V_d} \quad \frac{1}{5} \tag{4.80}$$

$$H_{a4} \quad \frac{1}{5} 1 \quad M_{a4} \tag{4.85}$$

$$H_{a3} \quad \frac{1}{5} 1 \quad M_{a3} \tag{}$$

$$v_{ao} \quad H_{aN}V_{N0} \quad H_{aN\ 1}V_{N\ 10} \quad \ldots \quad H_{a1}V_{10} \qquad (4.90) \qquad 0$$

$$v_{bo} \quad H_{bN}V_{N0} \quad H_{bN\ 1}V_{N\ 10} \quad \ldots \quad H_{b1}V_{10}$$

By substituting all the sharing functions to be unity, the switching functions are obtained as

$$H_{aN} \quad \frac{N \quad 1\, v_{ao}}{NV_d} \quad \frac{1}{N} \qquad H_{bN} \quad \frac{N \quad 1\, v_{bo}}{NV_d} \quad \frac{1}{N} \qquad H_{cN} \quad \frac{N \quad 1\, v_{co}}{NV_d} \quad \frac{1}{N}$$

$$H_{aN\ 1} \quad \frac{N \quad 3\, v_{ao}}{NV_d} \quad \frac{1}{N}$$

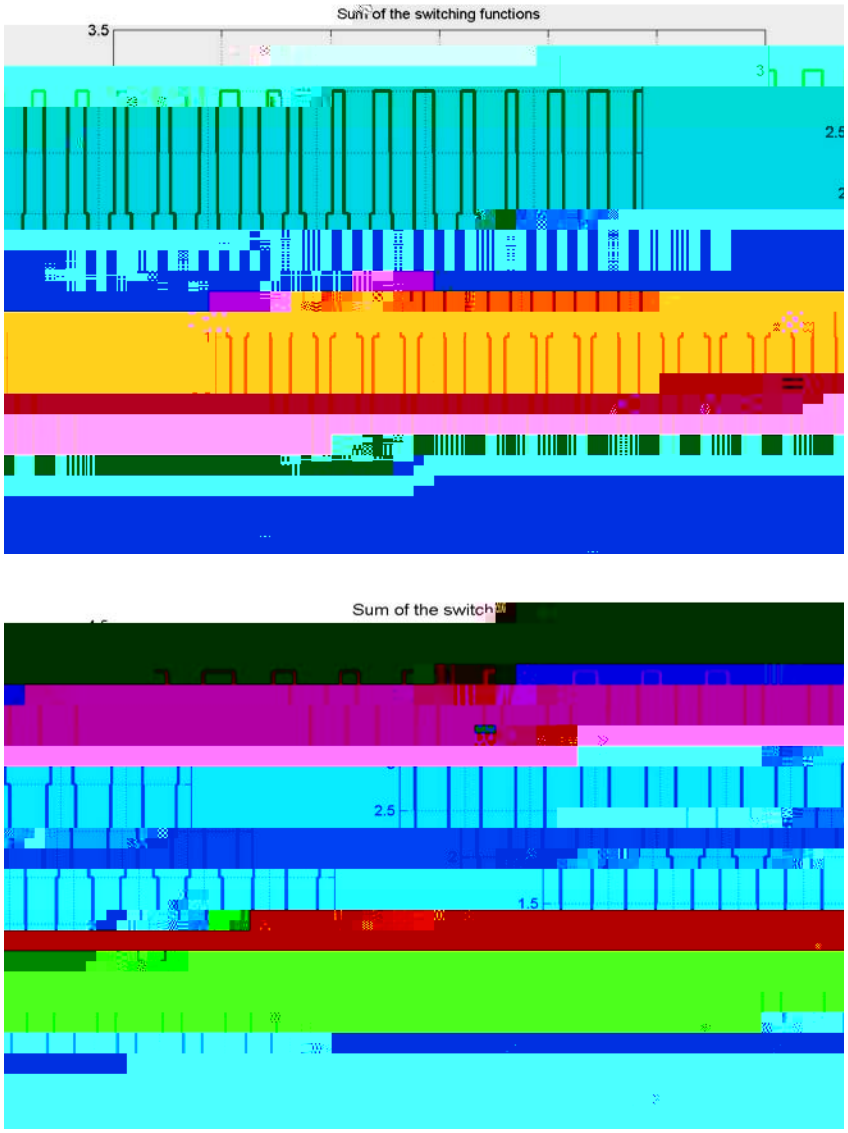


Figure 4.6: Sum of the switching functions

There some limitations in the scheme proposed:

There is shorting between the devices of the leg; i.e., the input side capacitors are getting shorted which is not acceptable.

Every time the voltage switches from zero to the node voltage it is connected and hence the entire voltage is impressed across the devices and hence high rating devices have to be used.

The main drawback of the single carrier-based method was the shorting problem; to overcome this problem, the conventional (N-1) carrier waveforms and single modulation signal is used. In this section, the equivalence of the single carrier and multiple carrier-based PWM technique is presented.

The output voltage of a three-level inverter is given by

$$H_{a3}V_{c1} \quad H_{a1}V_{c2} \quad V_{a0} \quad V_{02} \tag{4.97}$$

$$H_{b3}V_{c1} \quad H_{b1}V_{c2} \quad V_{b0} \quad V_{02} \tag{4.98}$$

$$H_{c3}V_{c1} \quad H_{c1}V_{c2} \quad V_{c0} \quad V_{02}. \tag{4.99}$$

Transforming the above equation to synchronous reference frame by using transformation matrix $T(\ )$, where

$$T(\ ) \quad \frac{2}{3} \begin{matrix} \cos(\ ) & \cos(\ \ \frac{2}{3}) & \cos(\ \ \frac{2}{3}) \\ \sin(\ ) & \sin(\ \ \frac{2}{3}) & \sin(\ \ \frac{2}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{matrix} \tag{4.100}$$

$_e dt$ $_0$; $_0$ - Initial reference angle.

The qd equations are obtained as

$$V_q^{\ e} \quad V_{c1} H_{q3} \quad V_{c2} H_{q1} \tag{4.101}$$

1 3 2 1

$$V_{d\ q}' \quad V_{c1}H_{q3} \quad V_{c2}H_{q1} \tag{4.110}$$

$$V_{d\ d}' \quad V_{c1}H_{d3} \quad V_{c2}H_{d1}. \tag{4.111}$$

Assuming

$$H_{q3} \qquad H_q \ ; \ H_{q1} \qquad H_q \tag{4.112}$$

d d

The modulation signals are obtained as

$$H_{a3} \quad \frac{V_d}{V_{c1} \quad V_{c2}} \quad _q \cos(\ ) \quad _d \sin(\ ) \quad H_{o3} \tag{4.119}$$

$$H_{b3} \quad \frac{V_d}{V_{c1} \quad V_{c2}} \quad _q \cos(\quad \frac{2}{3}) \quad _d \sin(\quad \frac{2}{3}) \quad H_{o3} \tag{4.120}$$

$$H_{c3} \quad \frac{V_d}{V_{c1} \quad V_{c2}} \quad _q \cos(\quad \frac{2}{3}) \quad _d \sin(\quad \frac{2}{3}) \quad H_{o3} \tag{4.121}$$

$$H_{a1} \quad \frac{V_d}{V_{c1} \quad V_{c2}} \quad _q \cos(\ ) \quad _d \sin(\ ) \quad H_{o3} \tag{4.122}$$

$$H_{b1} \quad \frac{V_d}{V_{c1} \quad V_{c2}} \quad _q \cos(\quad \frac{2}{3}) \quad _d \sin(\quad \frac{2}{3}) \quad H_{o1} \tag{4.123}$$

$$H_{c1} \quad \frac{V_d}{V_{c1} \quad V_{c2}} \quad _q \cos(\quad \frac{2}{3}) \quad _d \sin(\quad \frac{2}{3}) \quad H_{o1} \tag{4.124}$$

$$H_{a2} \quad 1 \quad H_{a1} \quad H_{a3} \tag{4.125}$$

$$H_{b2} \quad 1 \quad H_{b1} \quad H_{b3} \tag{4.126}$$

$$H_{c2} \quad 1 \quad H_{c1} \quad H_{c3}. \tag{4.127}$$

Assuming

$$X \quad \frac{V_d}{V_{c1} \quad V_{c2}} \text{ and } Y \quad \frac{V_d}{V_{c1} \quad V_{c2}} \tag{4.128}$$

where X and Y are the modulation indices of the signals in Eqs. (4.119) and (4.122).

In case of two triangle carrier-based technique, , decides the peaks of the two carriers and the sum of the two control variables must be equal to two; i.e., 2. The upper carrier waveform ranges from [1 – 1] and the lower carrier waveform

ranges from

Table 4. 1 illustrates the relation between the carrier waveform peaks and the modulation signal peaks. Consider 1, 1; substituting these values in Eq. (4.128), the modulation indices can be calculated. It can be seen from table 4.1 that the indices are 1 and –1. This is equivalent to the peaks of the triangles in the multiple carrier-based PWM. Similarly for different values of , the relation is obtained. It is clear that by varying the modulation signals is equivalent to varying the peaks of the triangle waveforms.

positive node voltage. With a three-phase three-level voltage source inverter there are 27 feasible switching modes. Obeying KVL and KCL the generated states are enumerated in Table 4.2. The inverter has 24 active states and three null states. A null state is defined as a state that does not contribute to the generation of the reference voltage. In this state the converter is connected to the same node in all the three phases. By controlling the duty cycles of devices in these zero states, the capacitors can be charged and discharged without contributing to the actual voltage.

	0 - H_{a0}	0- H_{a0}	0- H_{a0}	0-H_{a0}											

The next step in the modulation scheme is to find the equivalent voltages generated in each state. The voltages generated are expressed in the stationary reference frame. The qdo voltages of all the switching modes, also given in Table 4.3, are expressed in complex variable form as

$$v_{qds} \quad \frac{2}{3} v_{an} \quad a v_{bn} \quad a^2 v_{cn} \tag{4.129}$$

$$V_o \quad \frac{1}{3} v_{an} \quad v_{bn} \quad v_{cn} \tag{4.130}$$

where $a \quad e^{j}$, $\quad 120^0$.

The voltage space vectors of a three-phase converter are always located in the plane, and that is how they are represented in Figure 4.8. The space vector is comprised of 24 sectors of which the sector numbered from 1 – 6 are inner hexagon sectors and sector from 7 – 24 are outer hexagon. In general for a N-level converter, the space vector diagram has (N^3 – N) sectors. The number of hexagons increases as the number of levels increase. For a N-level converter, there are (N-1) hexagons.

As seen from Figure 4.8, the space vector has two hexagons, inner and outer hexagons, formed by 19 vectors. These 19 vectors are combined to form the 24-sector space vector. Naming the switching states with the numbers is much more general (applicable for any level) in which 2, 1, 0, where 2 means that the converter is connected to the positive voltage node, 1 represents the neutral point, and 0 connects to the negative node voltage. Out of the 19 vectors, the vectors corresponding to the inner sectors 1 – 6 are called the small vectors. Also in the inner hexagon there are some redundant vectors at the corners and these redundant vectors synthesize the same reference voltage but they have different zero sequence voltage. Also the currents in these states will be in the opposite directions and hence careful division of time intervals between these states can control the neutral current and the neutral point voltage. The vectors corresponding to the sectors from 7 – 12 are called the medium vectors. During the switching of these vectors the current has only one direction depending on the neutral point voltage. Hence the only vectors, which generate the neutral current, are the medium vectors. Vectors corresponding to the sectors 13 – 24 are known as the large vectors. These vectors do not contribute to the neutral current.

A reference signal V can be defined from the space vector using the vectors. Assuming that T

imposing the desired reference vector may be achieved by switching between these states. The nearest three vectors [NTV] concept is being used to divide the time between the states; i.e., the nearest three vectors that are close to the reference vector are determined and the turn on times of the states of the devices are determined depending on the control.

From Figure 4.8 assuming V_{qd}^{*} to be lying in sector k, the vectors are named a, b, c. In order to obtain optimum harmonic performance and minimize the switching losses, the state sequence is arranged such that switching only one inverter leg performs the transition from one state to the next. The central part of the space vector modulation strategy is the computation of switching times of the sectors for each modulation cycle. In the direct digital PWM method, the complex plane stationary reference frame qd output voltage vector of the three-phase voltage source inverter is used to calculate the turn-on times of the switches required to synthesize the reference voltage. In general, the three-phase balanced voltages expressed in the stationary reference frame, situated in the appropriate sector in Figure 4.8 are approximated by the time average over a sampling period of the three vectors. If the normalized times (with respect to modulator sampling time or converter switching period, T_s) of three vectors termed as V_{qda}, V_{qdb}, V_{qdc} corresponds to time signals t_a, t_b, and t_c, respectively, then the q and d components of the reference voltage V_{qd}^{*} are approximated as

$$V_{qd}^{*} \quad V_{qq} \quad jV_{dd} \quad V_{qda}t_a \quad V_{qdb}t_b \quad V_{qdc}t_c \tag{4.131}$$

and the devices have to switch according to the following constraint

$$t_a \quad t_b \quad t_c \quad 1. \tag{4.132}$$

Separating the real and imaginary terms in Eqs. (4.131)

$$V_{qq} \quad V_{qa} \quad V_{qc} \quad t_a \quad V_{qb} \quad V_{qc} \quad t_b \quad V_{qc}$$

$$V_{dd} \quad V_{da} \quad V_{dc} \quad t_a \quad V_{db} \quad V_{dc} \quad t_b \quad V_{dc} .$$

Expressing the above equations in the matrix form

$$\begin{matrix} qa & qc & qb & qc & a & qc \\ da & dc & db & dc & b & dc \end{matrix}$$

The voltages for the three vectors that correspond to sector 1 are

$$V_{qa} \quad \frac{V_d}{6}; V_{da} \quad \frac{V_d}{2\sqrt{3}}$$

$$V_{qb} \quad \frac{V_d}{3}; V_{da} \quad 0$$

$$V_{qc} \quad 0; V_{dc} \quad 0.$$

Hence by substituting the above known terms in Eqs. (4.133)-(4.134), the turn on times of the devices is obtained as

$$t_a \quad \frac{0.5}{V_d}[3V_{qq} \quad \sqrt{3}V_{dd}]$$

$$t_b \quad \frac{\sqrt{3}V_{dd}}{V_d}.$$

Hence in the similar way in each sector the turns on times of the devices are calculated and are enlisted in Table 4.4. These timings are in terms of the reference qd voltages.

Thus the mentioned procedure is used for microprocessor or DSP-based implementation of the space vector PWM [33-40]. The state diagram corresponding to each sector is drawn and the pattern has to be loaded into the DSP to turn on the devices. Figure 4.9 shows the state diagram for sector 1. In space vector the states have to be sequenced to obtain minimum switching but this sequencing is not necessary in the carrier-based PWM technique. The technique is explained in the following section.

1	$\frac{0.5}{V_d}[3V_{qq} \quad \sqrt{3}V_{dd}]$	$\frac{\sqrt{3}V_{dd}}{V_d}$

15	$\frac{3V_{qq}}{V_d}$	$\frac{\sqrt{3}}{V_d}[\sqrt{3}V_{qq} \quad V_{dd}]$
16	$\frac{\sqrt{3}}{V_d}[\sqrt{3}V_{qq} \quad V_{dd}]$	$\frac{3V_{qq}}{V_d}$

17 0 50.59 0 7.0036 424.02 585 592.08 Tm(])Tj12.0063 0 0 12.0063 267.4806 59CQ34

(222(+), 111(0), 000(-)). The variable is used to divide the time interval t_c between the positive (222) and zero vector (000) or the negative (111) and the zero vector (000). The vectors corresponding to 1A are U_a (221), U_a (211), and U_c(000, 111). The time for which the devices corresponding to sector 1A are turned on is shown in Table 4.5 as the existence functions.

	H_{a1}	H_{a2}	H_{a3}	H_{b1}	H_{b2}	H_{b3}	H_{c1}	H_{c2}	H_{c3}
1A	0	$t_a+t_b+ t_c$	t_c	t_c	$t_c+t_a+t_b$	0	$t_b+ t_c$	t_c+t_a	0
1B	0	$t_b+ t_c$	t_c+t_a	0	$t_a+t_b+ t_c$	t_c	t_c	$t_c+t_a+t_b$	0

In the carrier-based implementation of the space vector modulation, the equivalent modulation signals are determined for the timing expression using the space vector principle such that when the modulation signal is compared with the carrier waveform turns on the device for the same amount of time. Hence in a way the sine-triangle and the space vector modulation are exactly equivalent in every way [76-77]. In the carrier- based implementation, the Phase Disposition (PD) technique is used. Figure 4.7 shows the reference and the carrier waveform arrangements required to achieve this form of modulation for three-level inverter. In Figure 4.1 the important criteria to satisfy KVL and KCL is

$$H_{a3} \quad H_{a2} \quad H_{a1} \quad 1$$

$$H_{b3} \quad H_{b2} \quad H_{b1} \quad 1$$

$$H_{c3} \quad H_{c2} \quad H_{c1} \quad 1$$

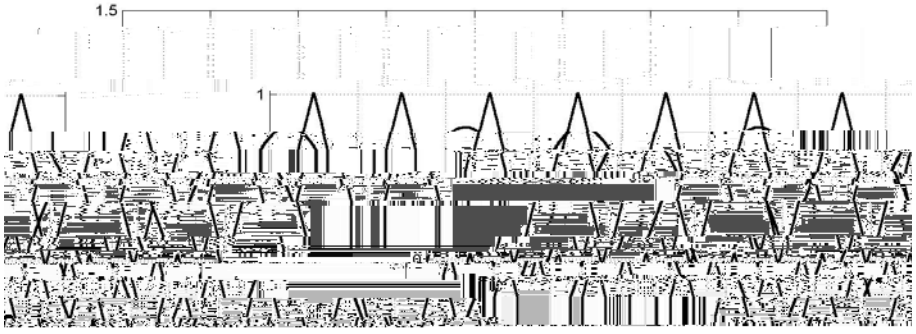


Figure 4.11: Carrier-based PWM using the phase disposition technique.

where H_{ij} are switching functions and are defined as when compared with two triangles equally displaced.

$$V_{abc} \quad Triangle \quad 1 \quad \&$$
$$Triangle \quad 2; \; H_{i3} \quad 1; \; otherwise \quad H_{i3} \quad 0$$

$$V_{abc} \quad Triangle \quad 1 \quad \&$$
$$Triangle \quad 2; \; H_{i2} \quad 1; \; otherwise \quad H_{i2} \quad 0$$

$$V_{abc} \quad Triangle \quad 1 \quad \&$$
$$Triangle \quad 2; \; H_{i1} \quad 1; \; otherwise \quad H_{i1} \quad 0$$

The phase voltage equations for star-connected, balanced three-phase loads expressed in terms of the existence functions and input nodal voltage V_{30}, V_{20}, V_{10} is given by Eqs. (4.1 - 4.3). The quantities v_{ao}, v_{bo}, v_{co} are the output voltages of the inverter with respect to the neutral point of the two capacitors. V_{20} is the neutral voltage which is floating between the neutral of the load and the neutral point of the two capacitors. This voltage may assume any value and hence becomes a part of the control.

The stationary reference frame qdo voltages of the switching modes, also given in Table 4.2 are expressed as

$$f_q \quad - \quad f_a \quad f_b \quad f_c$$

timing expression in terms of the reference line-line voltages. Hence the timing expressions, which are in terms of the qd voltages, are transformed to abc reference frame.

The stationary reference frame inverse transformation is given as

$$f_a \quad f_q \quad f_o$$

$$f_b \quad \frac{f_q}{2} \quad \frac{\sqrt{3}}{2} f_d \quad f_o$$

$$\_\_ \quad \sqrt{\ }$$

$\frac{v_{ab} \quad 2v_{cb}}{V_d}$	
$\frac{v_{ca}}{V_d}$	

$\frac{[v_{ac}}{V_d}$	